

177

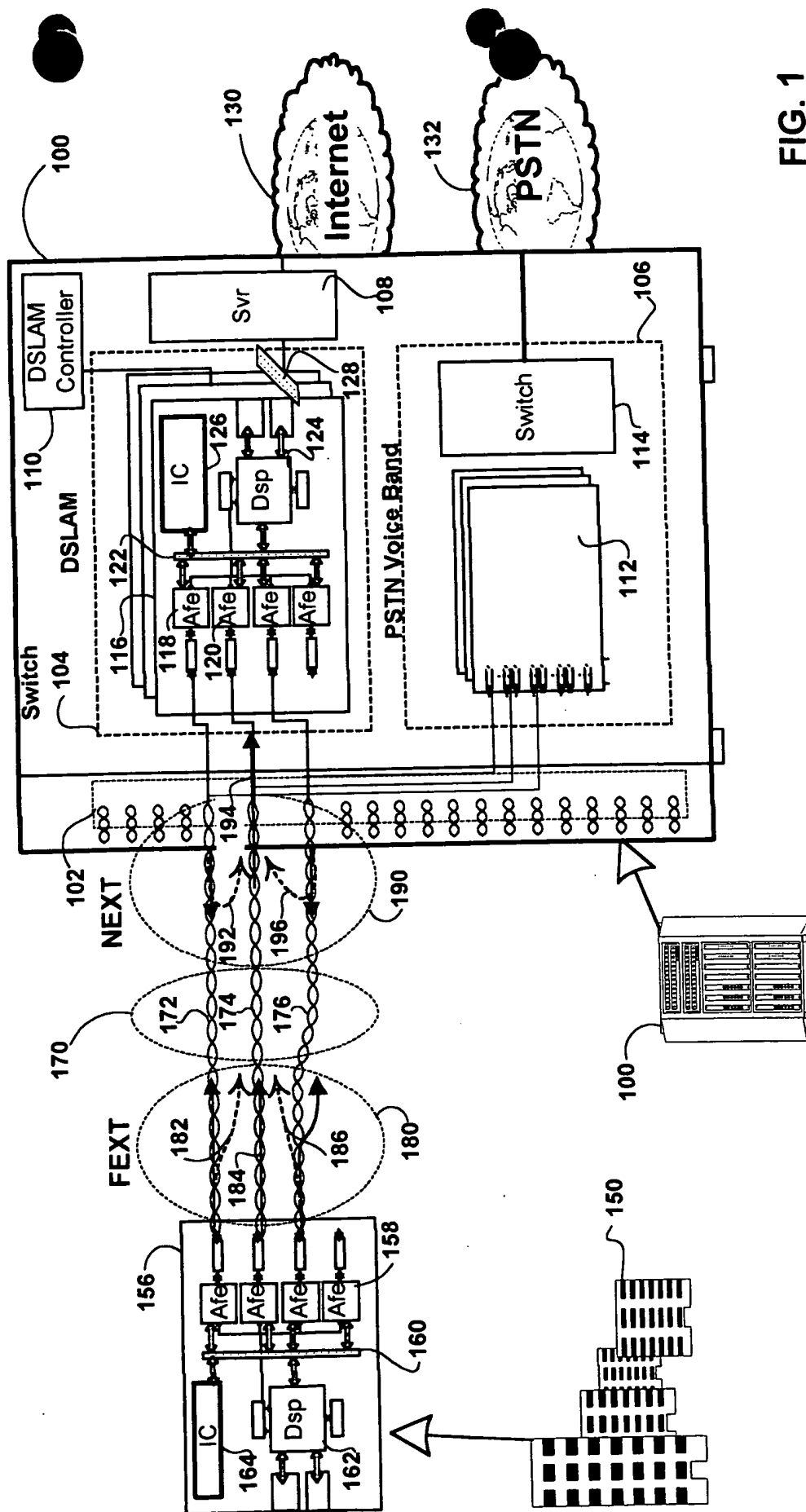


FIG. 1

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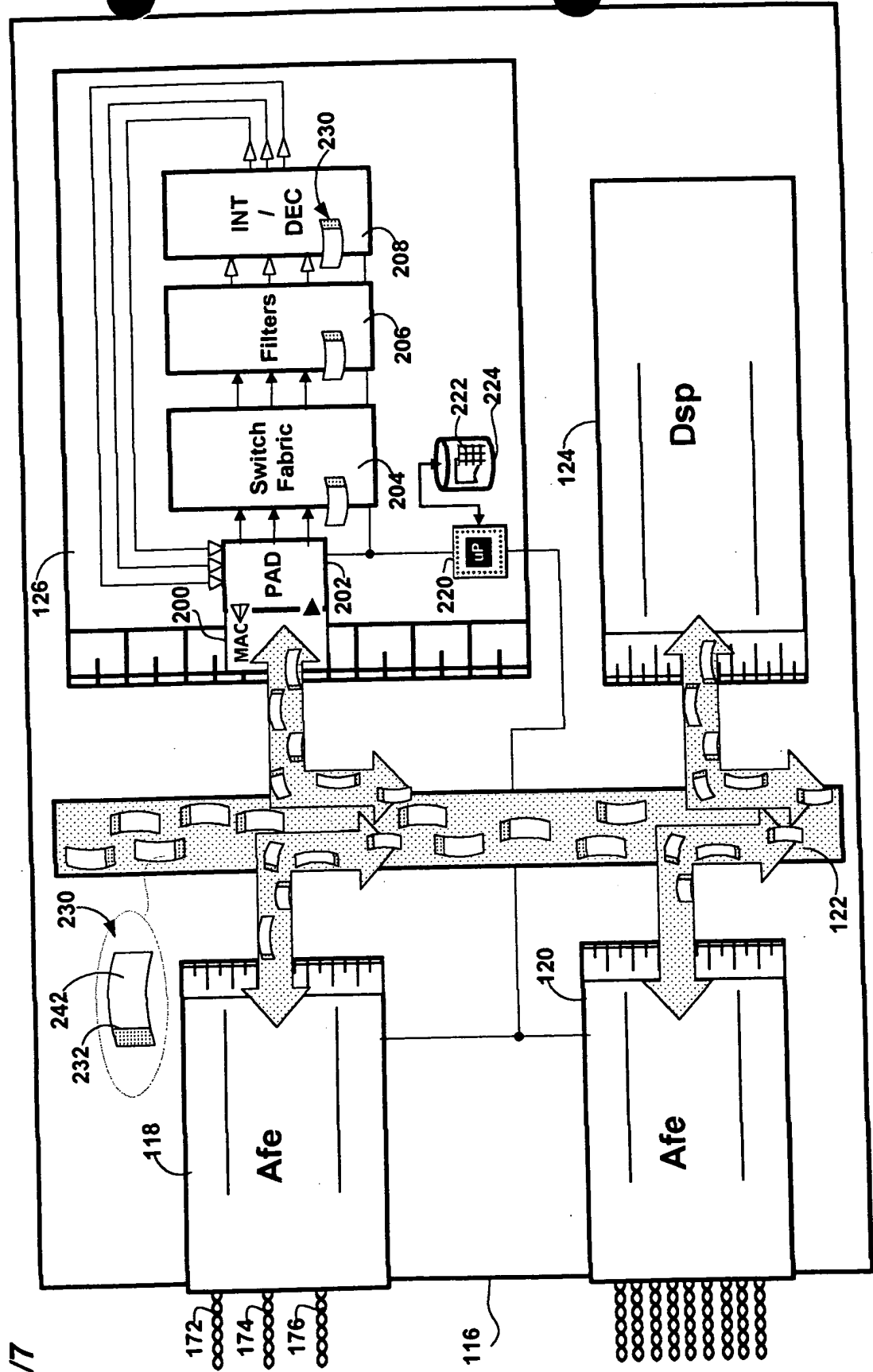


FIG. 2

FIG. 3

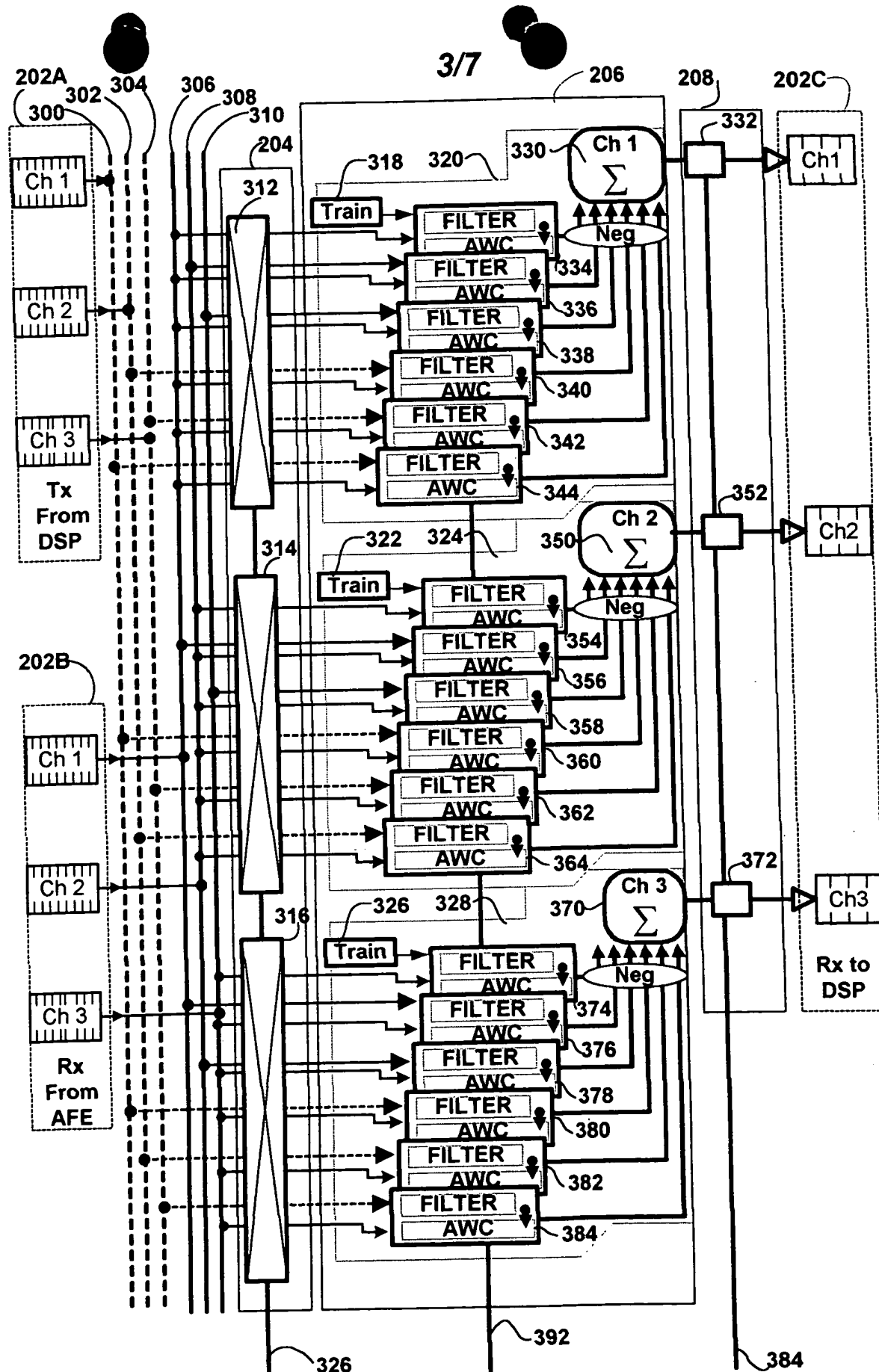


FIG. 3

FIG. 4 is a block diagram of a digital filter system. The system includes a coefficient generator (410) that provides coefficients (414, 416, 418, 420) to a series of multipliers (432, 436, 440, 444). The input signal (400) is processed through a series of adders (434, 438, 442, 446) and FIFO buffers (430, 432, 434, 436, 438, 440, 442, 444) to produce the output signal (404). The output signal (404) is also fed back to a summer (330) which produces the error signal (e(n)).

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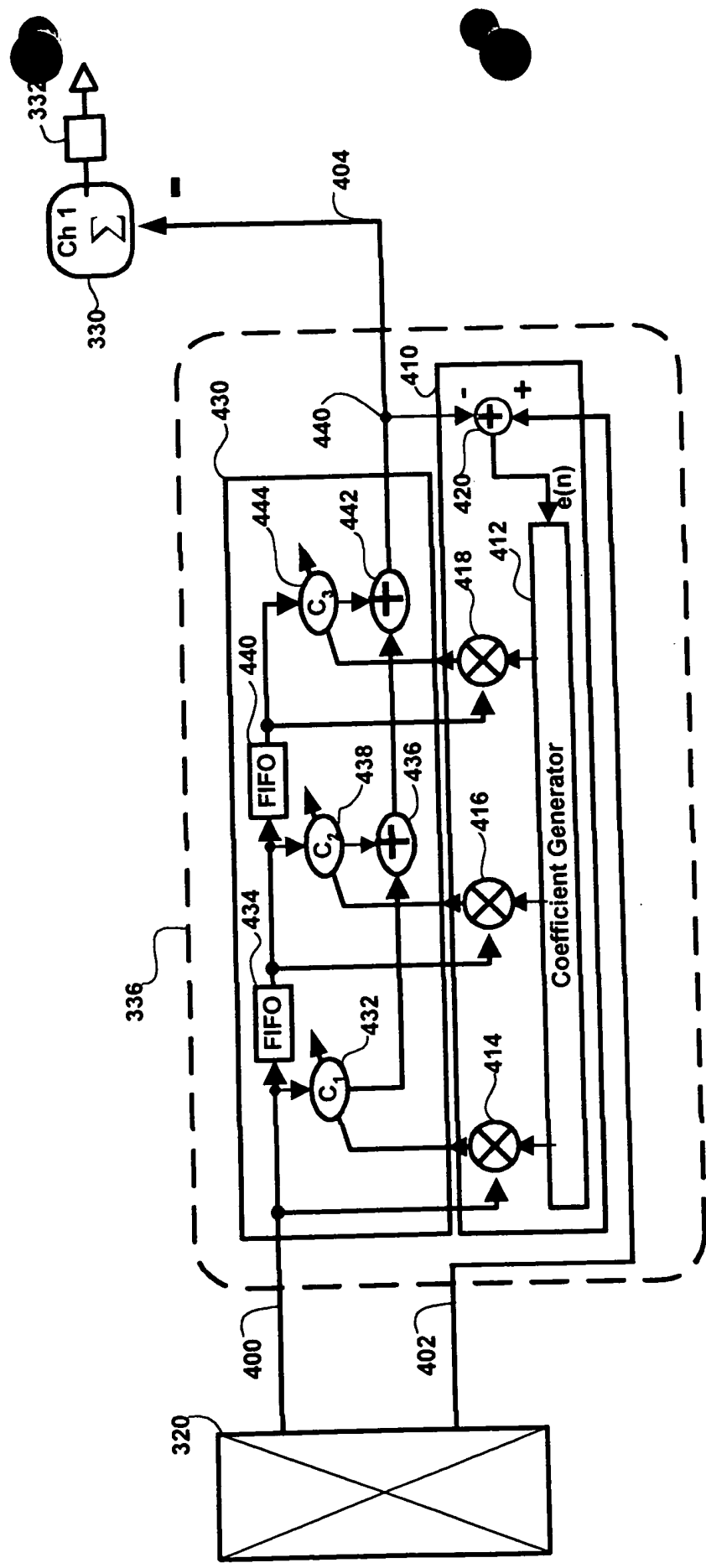


FIG. 4

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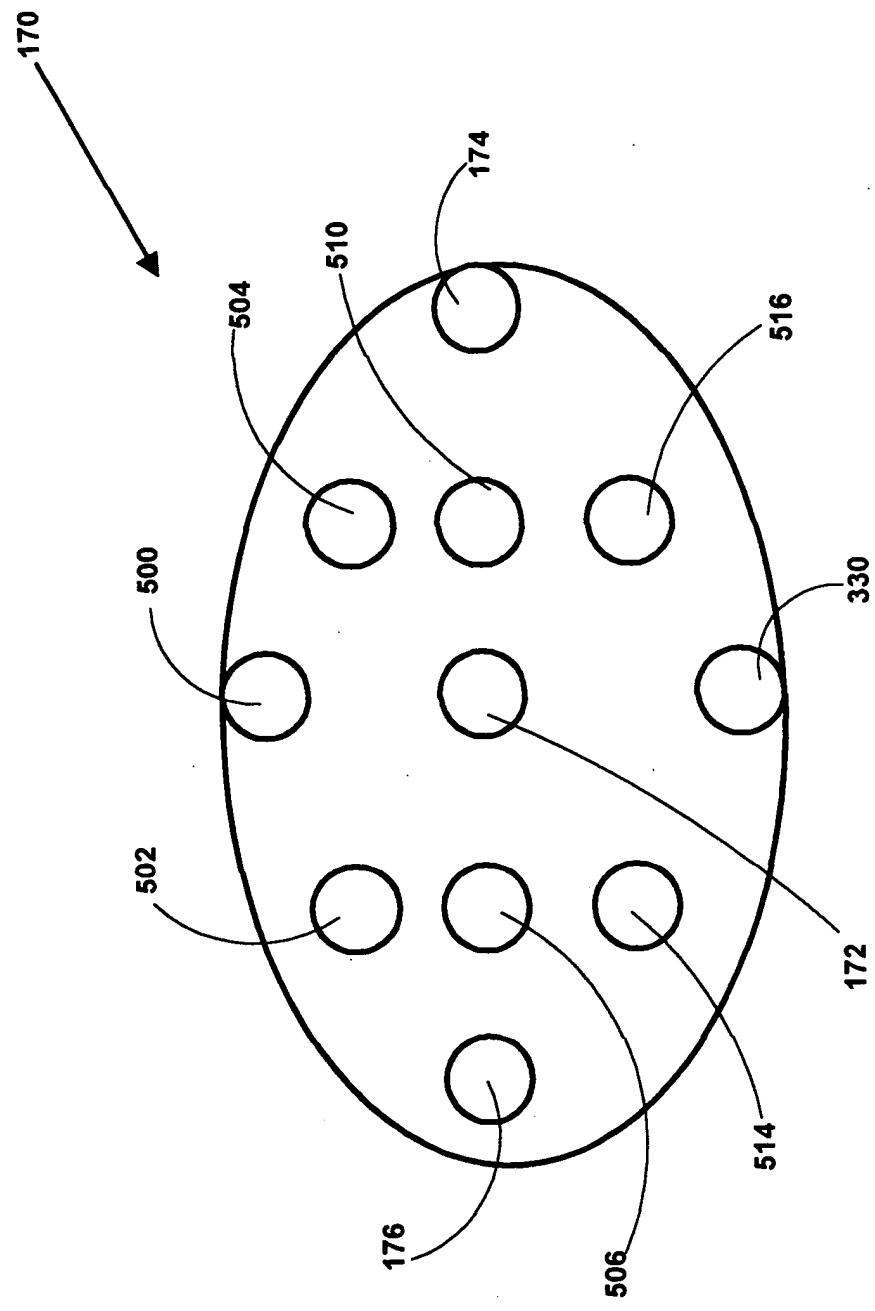


FIG. 5

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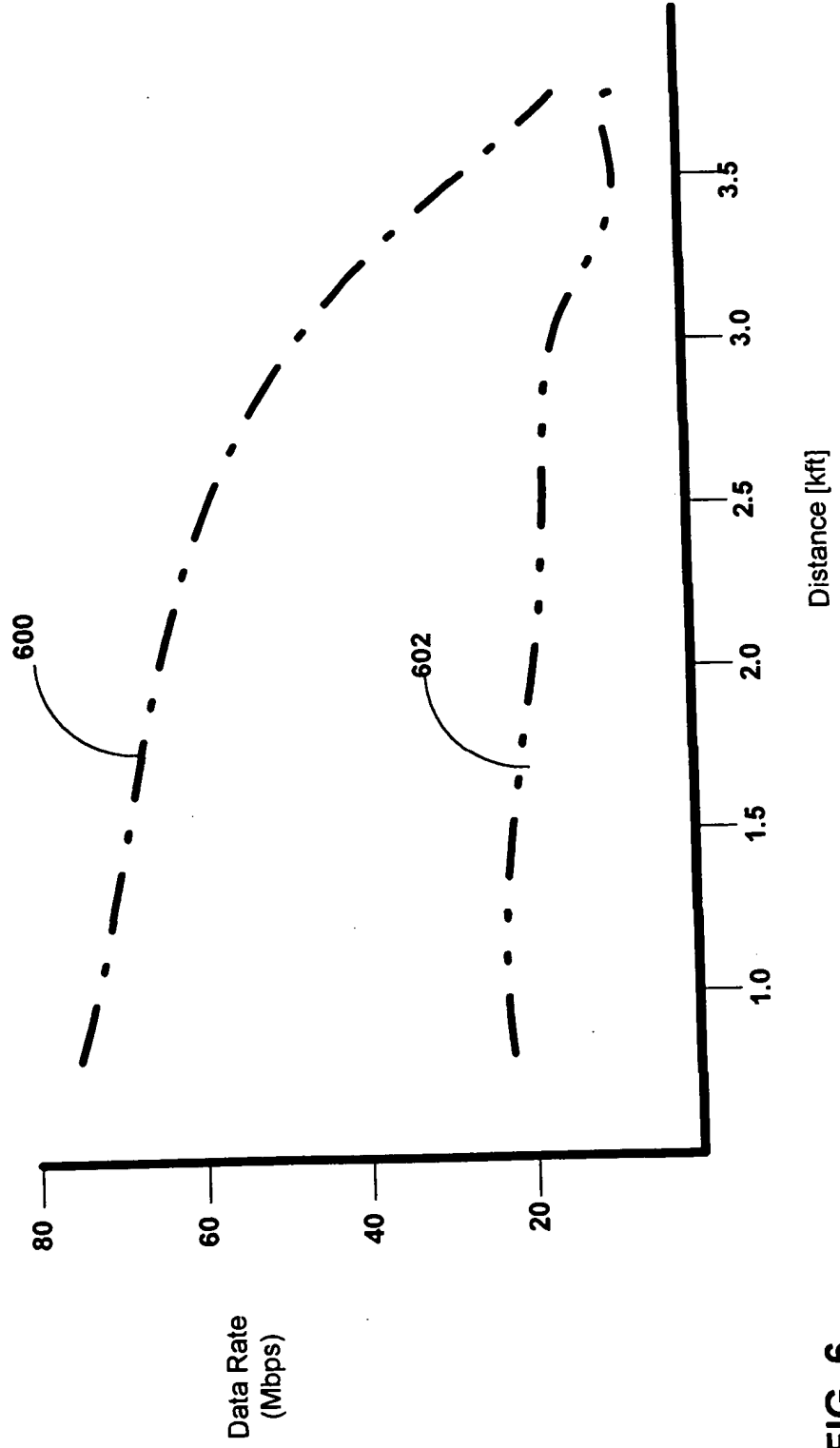


FIG. 6

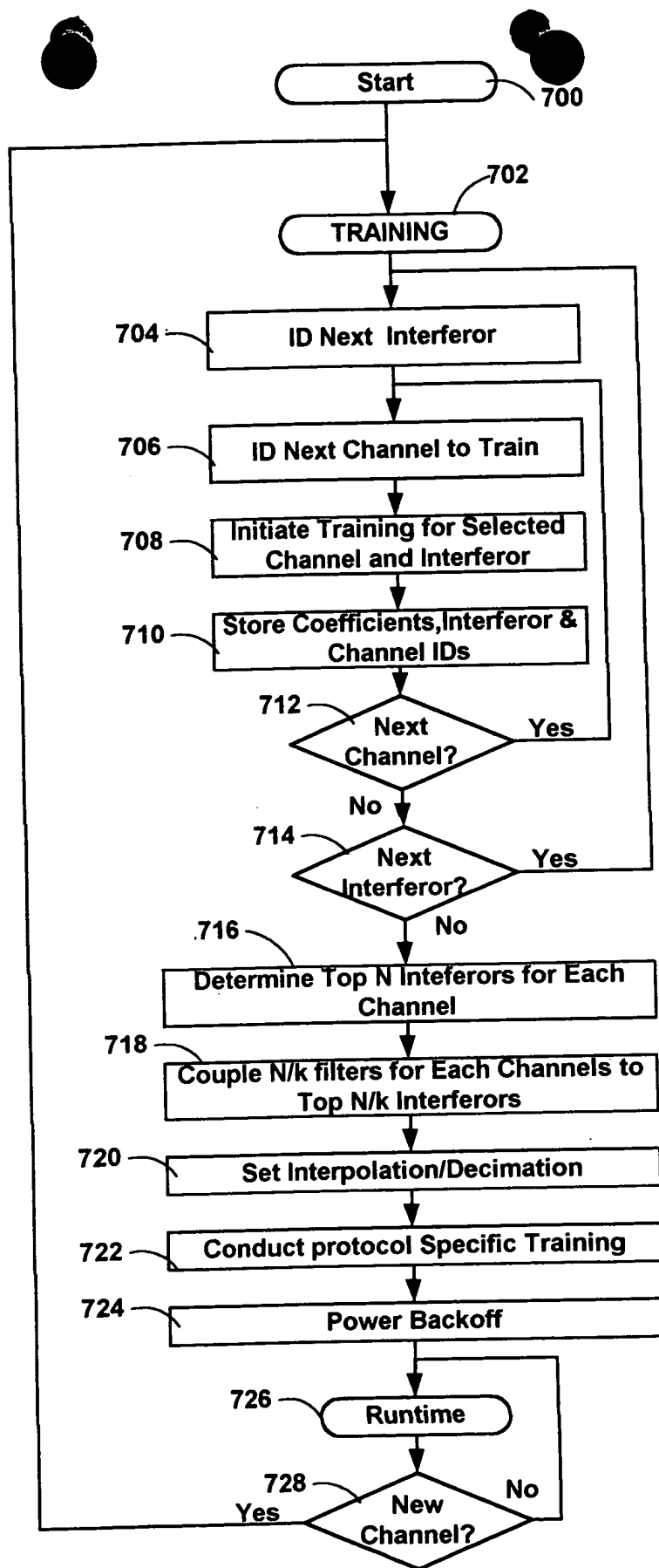


FIG. 7